AMENDMENTS TO THE CLAIMS

(IN REVISED FORMAT COMPLIANT WITH THE PROPOSED

REVISION TO 37 CFR 1.121)

1. (CURRENTLY AMENDED) An apparatus comprising:

a phase lock loop (PLL) configured to multiply an input frequency to generate an output frequency in response to a multi-bit lock signal; and

a lock circuit configured to generate said multi-bit lock signal, wherein said PLL is configured to (i) (a) select a reference frequency as said input frequency and (b) select a first feedback ratio, when in a first mode and (ii) (a) select a divided frequency of said input frequency as said input frequency and (b) select a second feedback ratio, when in a second mode, wherein (i) said divided frequency is adjustable in response to said multi-bit lock signal, (ii) a first bit of said multi-bit lock signal selects said first feedback ratio, and (iii) a second bit of said multi-bit lock signal selects said second feedback ratio.

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2. (PREVIOUSLY AMENDED) The apparatus according to claim 1, wherein said first mode is further configured to increase said first feedback ratio.

3. (PREVIOUSLY AMENDED) The apparatus according to claim 2, wherein said second mode is further configured to decrease said second feedback ratio.

4. (ORIGINAL) The apparatus according to claim 1, wherein said lock circuit comprises a lock decision logic circuit.

5. (ORIGINAL) The apparatus according to claim 1, wherein said lock circuit comprises a timer circuit.

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6. (PREVIOUSLY AMENDED) The apparatus according to claim 1, wherein said lock signal is generated in further response to an internal/external signal.

7. (ORIGINAL) The apparatus according to claim 1, wherein said lock is controlled by a timer.

8. (PREVIOUSLY AMENDED) The apparatus according to claim 1, wherein said multi-bit lock is externally controlled by a user.

9. (ORIGINAL) The apparatus according to claim 1, wherein said PLL comprises:

a first switchable divider configured to generate a reference frequency in response to said input frequency;

a PLL logic circuit configured to generate said output frequency in response to said reference frequency and a feedback frequency; and

a second switchable divider configured to generate said feedback frequency in response to said output frequency.

10. (PREVIOUSLY AMENDED) The apparatus according to claim 9, wherein said first and second switchable dividers are further configured in response to said multi-bit lock signal.

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11. (PREVIOUSLY AMENDED) The apparatus according to claim 10, wherein:

said first switchable divider comprises a first divider and a first multiplexer, wherein said first multiplexer is configured to select a first divided output frequency or said input frequency as said reference frequency; and

said second switchable divider comprises a second divider, a third divider and a second multiplexer, wherein said multiplexer is configured to select a second divided output frequency or a third divided frequency as said feedback frequency.

12. (ORIGINAL) The apparatus according to claim 11, wherein said second and third dividers are configured in series.

13. (ORIGINAL) The apparatus according to claim 11, wherein said second and third dividers are configured in parallel.

14. (PREVIOUSLY AMENDED) The apparatus according to claim 11, wherein said second and third dividers comprise multi-channel dividers configured in response to said multi-bit lock signal.

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15. (CURRENTLY AMENDED) An apparatus comprising:

means for multiplying an input frequency in response to a lock signal;

means for generating an output frequency in response to said input frequency;

means for generating said lock signal; and

means for (i) (a) selecting said input frequency to be a reference frequency and (b) selecting a first feedback ratio, when in a first mode and (ii) (a) selecting a divided frequency of said input frequency to be said reference frequency and (b) selecting a second feedback ratio, when in a second mode, wherein (i) said divided frequency is adjustable in response to said multi-bit lock signal, (ii) a first bit of said multi-bit lock signal selects said

first feedback ratio, and (iii) a second bit of said multi-bit lock signal selects said second feedback ratio.

16. (CURRENTLY AMENDED) A method for frequency and/or phase acquisition in a phase lock loop (PLL), comprising the steps of:

(A) multiplying an input frequency in response to a lock signal;

(B) generating said lock signal;

(C) (i) (a) selecting said input frequency to be a reference frequency and (b) selecting a first feedback ratio, when in a first mode and (ii) (a) selecting a divided frequency of said input frequency to be said reference frequency and (b) selecting a second feedback ratio, when in a second mode, wherein (i) said divided frequency is adjustable in response to said multi-bit lock signal, (ii) a first bit of said multi-bit lock signal selects said first feedback ratio, and (iii) a second bit of said multi-bit lock signal selects said second feedback ratio.

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17. (PREVIOUSLY AMENDED) The method according to claim 16, wherein step (A) further comprises:

increasing said first feedback ratio when in said first mode; and

decreasing said second feedback ratio when in said second mode.

18. (PREVIOUSLY AMENDED) The method according to claim 16, wherein step (B) generates said lock signal in further response to an internal/external signal.

19. (ORIGINAL) The method according to claim 16, wherein step (A) further comprises:

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generating a reference frequency in response to said input frequency;

generating an output frequency in response to said reference frequency and a feedback frequency; and

generating said feedback frequency in response to said output frequency.

20. (ORIGINAL) The method according to claim 16, wherein step (A) further comprises:

selecting a first divided output frequency or said input frequency and presenting said reference frequency; and

selecting a second divided output frequency or a third divided frequency and presenting said feedback frequency.

21. (PREVIOUSLY NEW) An apparatus comprising:

a phase lock loop (PLL) configured to multiply an input frequency to generate an output frequency in response to a lock signal; and

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a lock circuit configured to generate said lock signal in response to an external input, wherein said PLL is configured to (i) select a reference frequency as said input frequency when in a first mode and (ii) select a divided frequency of said input frequency as said input frequency when in a second mode, wherein either said first mode or said second mode is selected in response to said lock signal.